**Preliminary Information**

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

# Bt8921

## *HDSL Analog Front End (AFE)*

Brooktree's HDSL Analog Front End (AFE) greatly reduces the size and cost of an HDSL system by providing all of the active analog circuitry needed to connect the Brooktree Bt8952 HDSL digital signal processor to a 1:2 HDSL line transformer. Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the twisted pair line and passes it to the Bt8952. The HDSL analog interface is a monolithic device fabricated on a 0.6 micron CMOS. It operates on a single +5 V supply (using only 300 mW), and is housed in a 48-pin SSOP package.

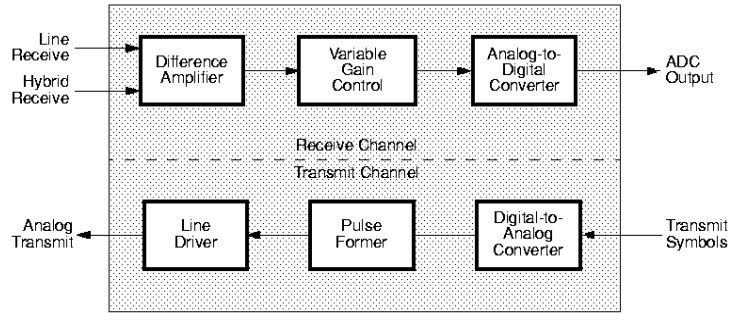
The receive channel is designed around an analog-to-digital converter. It includes a difference amplifier that can be used with an external hybrid for first order echo cancellation. A programmable gain amplifier, controlled by the Bt8952, is also included to accommodate varying line attenuation. The analog-to-digital converter produces 13 bits of resolution with ±1 LSB integral linearity at output rates up to 584,000 symbols per second.

The transmit channel consists of a switched-capacitor pulse-forming network followed by a differential line driver. The pulse-forming network receives symbol data from the XMIT and XMITB outputs of the Bt8952 and generates a 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 and ETR152, Bellcore Technical Advisory TA-NWT-001210, and ANSI Technical Report T1E1.4/94-006. The differential line driver uses a composite output stage combining class B operation (for high-efficiency driving of large signals) with class AB operation (to minimize crossover distortion). In addition to providing a low-impedance output, the line driver provides a smoothing filter function for the switched-capacitor pulse-former output. The device is second-sourced by Burr Brown Corporation as AFE1103E. This device operates at both T1 and E1 rates.

### Distinguishing Features

- Complete HDSL Analog Interface
- Single Chip Solution
- Supports E1 and T1 Data Rates
- Meets all Relevant HDSL Specifications
  - Bellcore TA-NWT-001210 (T1)
  - ANSI T1E1.4/94-006 (T1)
  - ETSI RTR/TM-03036 (E1)
  - ETSI ETR152 (E1)
- Low Power Dissipation: 300 mW
- Operates from a Single +5 Vdc Power Supply
- 48-Pin SSOP Package
- –40°C to +85°C Operation

### Functional Block Diagram

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## Ordering Information

| Order Number | Package | Ambient Temperature |
|---|---|---|
| Bt8921ESS | 48-pin Shrink Small Outline Package (SSOP) | –40° to +85° C |


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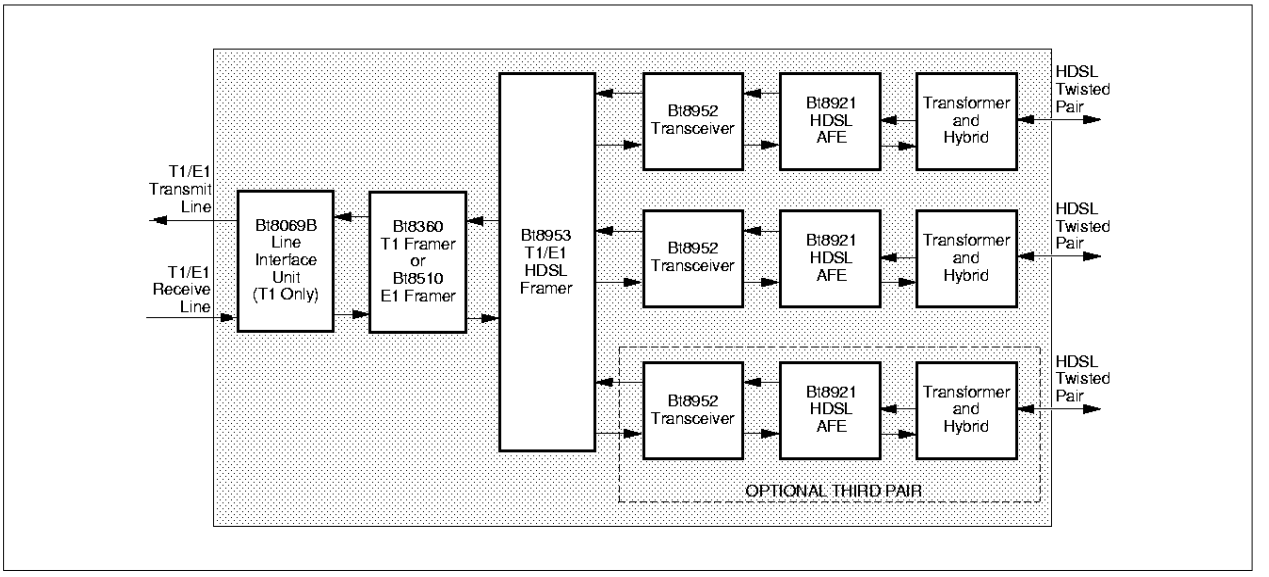
# System Overview

## HDSL System with Bt8921

The Bt8921 HDSL Analog Front End (AFE) is an integral component of Brooktree's HDSL chipset. System performance of the chipset allows 2-pair T1, 2-pair E1, and 3-pair E1 transmission. The major building blocks of a typical HDSL T1/E1 terminal are shown in Figure 1.

***Figure 1. HDSL T1/E1 Terminal***




The Bt8921 provides the interface between the analog and digital domains in the HDSL system. It performs all the active amplification, filtering, analog-to-digital, and digital-to-analog conversion needed to connect the Bt8952 transceiver to an HDSL line transformer. The Bt8952 transceiver performs adaptive echo cancellation, equalization, symbol quantization, and clock recovery. The Bt8953 channel unit is responsible for HDSL framing and overhead functions as well as multiplexing/demultiplexing of the two or three HDSL data streams to/from the primary-rate T1/E1 data stream.

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## Performance Summary

A summary of the Bt8921 performance characteristics is listed below in Table 1, Performance Summary.

***Table 1. Performance Summary** (1 of 3)*

| | Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Receive Channel | Receive Clock Rate, $f_{rx}$ (1) | 48 x TXCLK (TXCLK = Symbol rate) | TBD | | 28.032 | MHz |
| | T1 Mode | | | 18.816 | | MHz |
| | E1 Mode | | | 28.032 | | MHz |
| | Analog Inputs | Differential | | | | |
| | Hybrid Tip (RXHYB+) | G = +1 | | | | |
| | Hybrid Ring (RXHYB–) | G = –1 | | | | |
| | Line Tip (RXLINE+) | G = +1 | | | | |
| | Line Ring (RXLINE–) | G = –1 | | | | |
| | Input Voltage Range (2) | Balanced Differential | –3.5 | | +3.5 | V |
| | Input Impedance | All Inputs | | 40 | | kΩ |
| | Input Capacitance | | | TBD | | |
| | Input Matching | | | | ±2 | % |
| | Common Mode Voltage | | | Vdd/2 | | |
| | A/D Converter | | | | | |
| | Resolution | No Missing Codes | 13 | | | Bits |
| | Integral Linearity (3) | 13-bit LSB | | | ±1 | LSB |
| | Differential Linearity (3) | | | | ±0.8 | LSB |
| | Programmable Gain | Four gains between 0 dB and +9 dB | 0 | | +9 | dB |
| | Gain + Offset Error | | | 5 | | % FSR (4) |
| | Output Data Rate | $f_{rx}$/48 | | | | |
| | T1 mode | | | 392 | | kHz |
| | E1 mode | | | 584 | | kHz |
| | SINAD (5) | | 70 | | | dB |

***Table 1. Performance Summary** (2 of 3)*

| | Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Transmit Channel | Transmit Clock Rate, $f_{tx}$: | TXCLK Input | TBD | | 584 | kHz |
| | T1 Mode | | | 392 | | kHz |
| | E1 Mode | | | 584 | | kHz |
| | T1 Mode Operation: (6, 7) | | | | | |
| | Pulse Template (8) | See Figure 2 | | | | |
| | Power Spectral Density (9) | See Figure 3 | | | | |
| | –3 dB Point | | | 196 | | kHz |
| | Average Power(3, 9) | 0 to 784 kHz, $R_L$ = 65 Ω | 13 | | 14 | dBm |
| | E1 Mode Operation: (6, 10) | | | | | |
| | Pulse Template | See Figure 2 | | | | |
| | Power Spectral Density (9) | See Figure 3 | | | | |
| | –3 dB Point | | | 292 | | kHz |
| | Average Power (3, 9) | 0 to 1.168 MHz, $R_L$ = 65 Ω | 13 | | 14 | dBm |
| | Output Voltage Range | Balanced Differential, $R_L$ = 28 Ω | ±3.1 | ±3.3 | ±3.5 | V |
| | Output Current | | 125 | | | mA |
| | Common-Mode Voltage | | | $V_{DD}/2$ | | V |
| | Output Impedance (3) | DC to 1 MHz | | | 2 | Ω |
| | Linearity (11) | At Output Symbol Peak | | | 0.012 | %FSR (4) |
| | Harmonic Distortion | 3 kHz, 3.4 Volt Peak Sine Wave Output, $R_L$ = 28 Ω | | | –65 | dB |
| | HDSL Transformer Ratio | T1 or E1 Rates | 1:2 | | | |
| | PLL Frequency Change Range | | | 100 | | ppm |
| Digital Interface (3) | Input Levels | HCMOS and TTL Compatible | | | | |
| | Output Levels | HCMOS Drive Compatible | 10 | | | Loads |
| | RX Interface: | | | | | |
| | $t_{rx1}$ | RXDATA to RXSYNC Setup Time | 50 | | | ns |
| | $t_{rx2}$ | RXDATA to RXSYNC Hold Time | 10 | | | ns |
| | Tx Interface: | | | | | |
| | $t_{tx1}$ | TXCLK Period | 1.7 | | | µs |
| | $t_{tx2}$ | TXCLK Pulse Width | 50 | | | ns |
| | $t_{tx3}$ | TXCLK to TXDATA Edge Allowable Error | 0 | | 200 | ns |
| Power | Power Supply Voltage | Specification | | 5 | | V |
| | Power Supply Voltage | Operating Range | 4.75 | | 5.25 | V |
| | Power Dissipation | V = +5 VDC, $R_L$ = 65 Ω | | 300 | | mW |
| | PSRR | Power Supply Rejection | 65 | | | dB |

***Table 1. Performance Summary** (3 of 3)*

| | Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Package** | Number of Pins | Plastic, SSOP | | 48 | | Pins |
| **Temperature Range** | Operating (3) | | –40 | | +85 | °C |

Notes:
(1). Receive clock is synthesized on chip from TXCLK.
(2). Input voltage range when Variable Gain Amplifier (VGA) gain equals 0 dB. Input voltage range is reduced proportionally as VGA gain is increased.
(3). Guaranteed by design and characterization.
(4). FSR is Full Scale Range.
(5). Signal to noise plus distortion; production tested with full-scale 8 kHz and 250 kHz input @ 584 kHz output data rate.
(6). Measured on line side of HDSL transformer loaded with 135 Ω, unless otherwise specified.
(7). Bellcore TA-NWT-001210 and ANSI T1E1.4/94-006 compliant.
(8). Per ANSI T1E1.4/96-006 contribution T1E1.4/92-168.
(9). Measured with a pseudo-random code sequence of HDSL pulses.
(10).ETSI RTR/TM-03036 and ETSI ETR152 compliant.
(11).Linearity guaranteed by measuring voltage levels of each of the four symbol outputs.

**Typical Performance Curves at Output of HDSL Pulse Transformer**

The curves shown below are measured at the line output of the HDSL transformer. Typical at 25°C and Vsupply = +5 V, unless otherwise specified. See Figure 2, Table 2, and Figure 3.

*Figure 2. Transmitted Pulse Template Measured at HDSL Transformer Output*

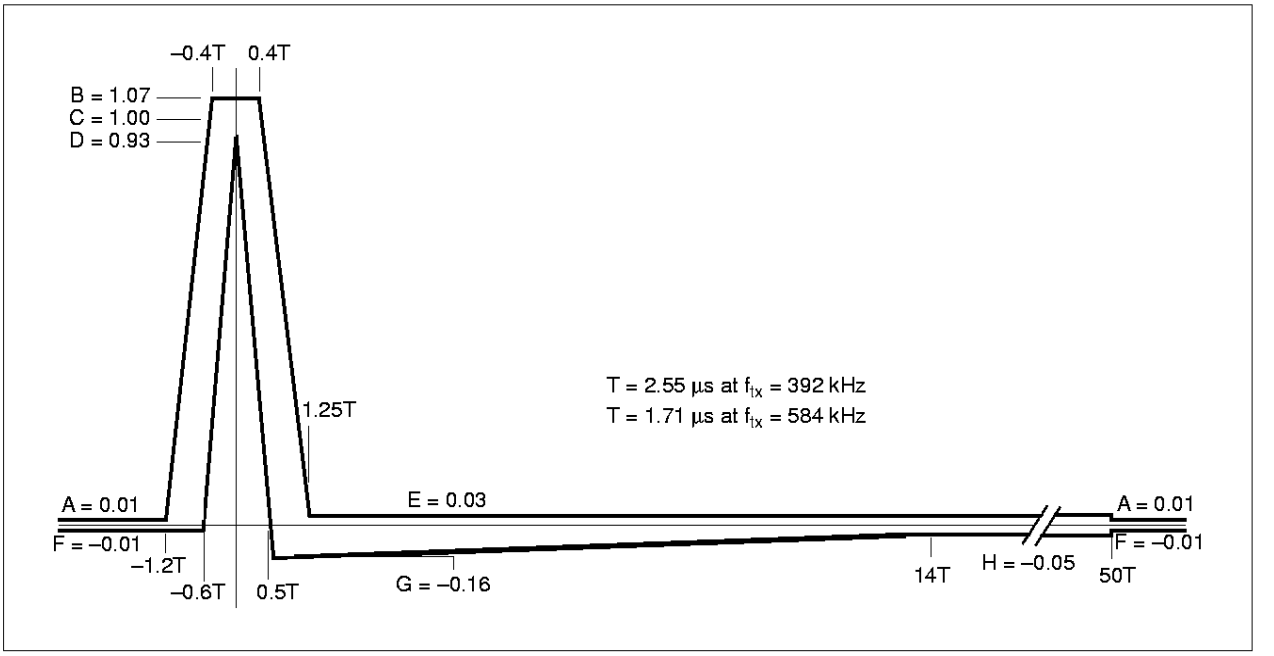
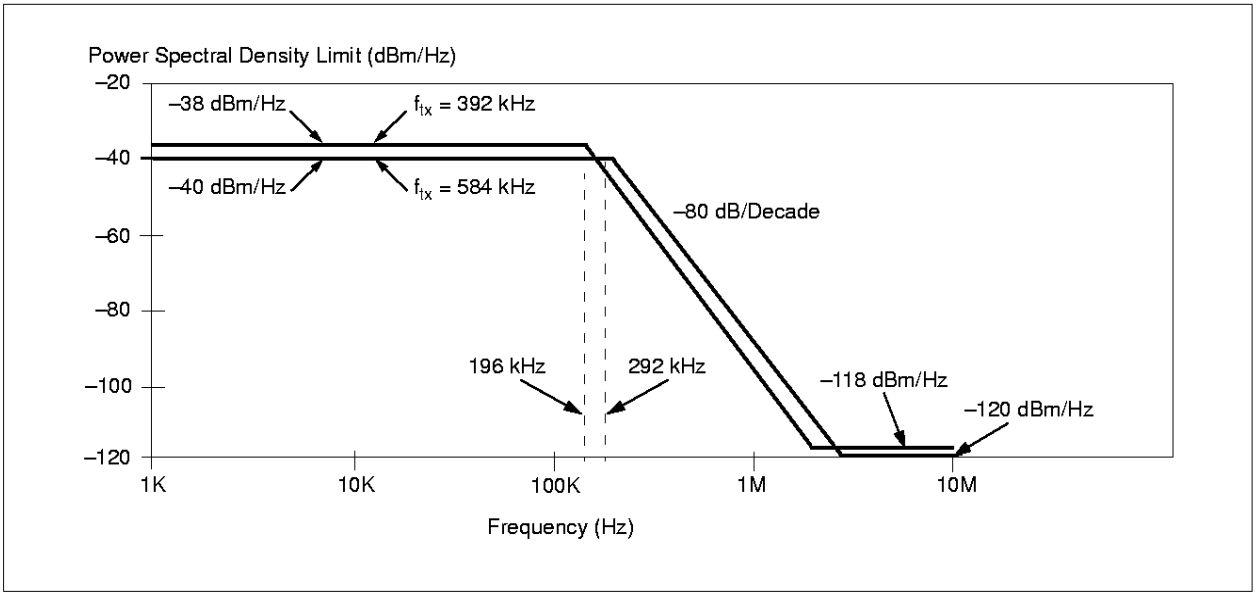



*Table 2. Transmitted Pulse Template Measured at HDSL Transformer Output*

| Normalized Level | | Quaternary Symbols | | | |
|---|---|---|---|---|---|
| | | +3 | +1 | –1 | –3 |
| A | 0.01 | 0.0264 | 0.0088 | –0.0088 | –0.0264 |
| B | 1.07 | 2.8248 | 0.9416 | –0.9416 | –2.8248 |
| C | 1.00 | 2.6400 | 0.8800 | –0.8800 | –2.6400 |
| D | 0.93 | 2.4552 | 0.8184 | –0.8184 | –2.4552 |
| E | 0.03 | 0.0792 | 0.0264 | –0.0264 | –0.0792 |
| F | –0.01 | –0.0264 | –0.0088 | 0.0088 | 0.0264 |
| G | –0.16 | –0.4224 | –0.1408 | 0.1408 | 0.4224 |
| H | –0.05 | –0.1320 | –0.0440 | 0.0440 | 0.1320 |

***Figure 3. Upper Bound of Power Spectral Density Measured at Output of HDSL Transformer***



# Pin Descriptions

Pin descriptions, numbers, names and types are listed in Table 3. A pinout diagram of the Bt8921 is illustrated in Figure 4.

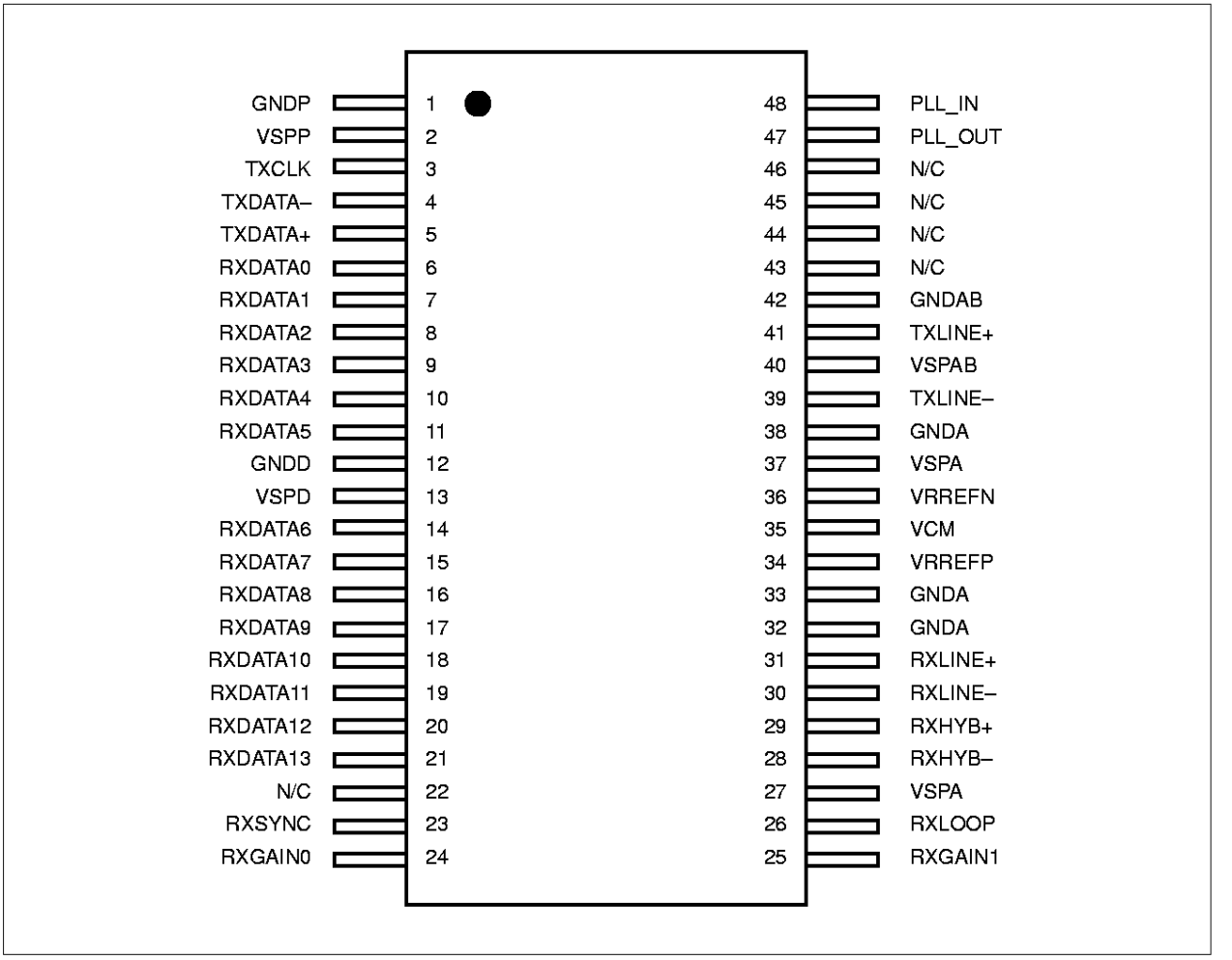
*Table 3. Bt8921 Pinout (1 of 2)*

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1 | GNDP | Ground | Analog ground for PLL |
| 2 | VSPP | Power | Analog supply (+5 V) for PLL |
| 3 | TXCLK | Input | Symbol clock (QCLK from Bt8952) (392 kHz for T1, 584 kHz for E1) |
| 4 | TXDATA– | Input | XMITB line from Bt8952 |
| 5 | TXDATA+ | Input | XMIT line from Bt8952 |
| 6 | RXDATA0 | Output | ADC output bit 0 (RCV 2 from Bt8952) |
| 7 | RXDATA1 | Output | ADC output bit 1 (RCV 3 from Bt8952) |
| 8 | RXDATA2 | Output | ADC output bit 2 (RCV 4 from Bt8952) |
| 9 | RXDATA3 | Output | ADC output bit 3 (RCV 5 from Bt8952) |
| 10 | RXDATA4 | Output | ADC output bit 4 (RCV 6 from Bt8952) |
| 11 | RXDATA5 | Output | ADC output bit 5 (RCV 7 from Bt8952) |
| 12 | GNDD | Ground | Digital ground |
| 13 | VSPD | Power | Digital supply (+5 V) |
| 14 | RXDATA6 | Output | ADC output bit 6 (RCV 8 from Bt8952) |
| 15 | RXDATA7 | Output | ADC output bit 7 (RCV 9 from Bt8952) |
| 16 | RXDATA8 | Output | ADC output bit 8 (RCV 10 from Bt8952) |
| 17 | RXDATA9 | Output | ADC output bit 9 (RCV 11 from Bt8952) |
| 18 | RXDATA10 | Output | ADC output bit 10 (RCV 12 from Bt8952) |
| 19 | RXDATA11 | Output | ADC output bit 11 (RCV 13 from Bt8952) |
| 20 | RXDATA12 | Output | ADC output bit 12 (RCV 14 from Bt8952) |
| 21 | RXDATA13 | Output | ADC output bit 13 (RCV 15 from Bt8952) |
| 22 | N/C | N/C | Connection to Ground recommended |
| 23 | RXSYNC | Input | A/D sync signal (RCVCLK) (392 kHz for T1, 584 kHz for E1) |
| 24 | RXGAIN0 | Input | Receive gain control bit 0 (AGAIN0 from Bt8952) |
| 25 | RXGAIN1 | Input | Receive gain control bit 1 (AGAIN1 from Bt8952) |
| 26 | RXLOOP | Input | Loopback control signal |
| 27 | VSPA | Power | Analog supply (+5 V) |

***Table 3. Bt8921 Pinout*** *(2 of 2)*

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 28 | RXHYB– | Input | Negative input from hybrid network |
| 29 | RXHYB+ | Input | Positive input from hybrid network |
| 30 | RXLINE– | Input | Negative line input |
| 31 | RXLINE+ | Input | Positive line input |
| 32 | GNDA | Ground | Analog ground |
| 33 | GNDA | Ground | Analog ground |
| 34 | VRREFP | Output | Positive reference output |
| 35 | VCM | Output | Common mode voltage (buffered) |
| 36 | VRREFN | Output | Negative reference output |
| 37 | VSPA | Power | Analog supply (+5 Volts) |
| 38 | GNDA | Ground | Analog ground |
| 39 | TXLINE– | Output | Negative line output |
| 40 | VSPAB | Power | Output buffer supply (+5 Volts) |
| 41 | TXLINE+ | Output | Positive line output |
| 42 | GNDAB | Ground | Output buffer ground |
| 43 | N/C | N/C | Connection to Ground recommended |
| 44 | N/C | N/C | Connection to Ground recommended |
| 45 | N/C | N/C | Connection to Ground recommended |
| 46 | N/C | N/C | Connection to Ground recommended |
| 47 | PLL_OUT | Output | PLL filter output |
| 48 | PLL_IN | Input | PLL filter input |

*Figure 4. Bt8921 48-pin Shrink Small Outline Package (SSOP) Pinout Diagram*



## Receive Channel Variable Gain Amplifier

The gain of the amplifier at the input of the receive channel is set by two gain control pins, RXGAIN1 and RXGAIN0. The resulting gain between 0 dB and +9 dB is shown in Table 4.

*Table 4. Receive Channel Variable Gain Settings*

| RXGAIN1 | RXGAIN0 | Gain |
|---|---|---|
| 0 | 0 | 0 dB |
| 0 | 1 | 3 dB |
| 1 | 0 | 6 dB |
| 1 | 1 | 9 dB |

## Receive Data Coding

The data from the receive channel A/D converter is coded in offset binary as listed in Table 5.

*Table 5. A/D Converter Output Format*

| Analog Input | Output Code (RXDATA[13:0]) |
|---|---|
| Positive Full Scale | 11111111111111 |
| Negative Full Scale | 00000000000000 |

## RXLOOP Input

RXLOOP is the loopback control signal. When enabled, the RXLINE+ and RXLINE– inputs are disconnected from the Bt8921. The RXHYB+ and RXHYB– inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to RXLOOP.

## Echo Cancellation

The RXHYB input is designed to be subtracted from the RXLINE input for first order echo cancellation. To accomplish this, note that the RXLINE input is connected to the same polarity signal at the transformer (+ to + and – to –) while the RXHYB input is connected to opposite polarity through the compromise hybrid (– to + and + to –) as shown in the Bt8921 Hybrid Configuration Diagram, Figure 9.

## Electrical Specifications

Stresses above those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

***Table 6. Absolute Maximum Ratings***

| Parameter | Value |
|---|---|
| Power Supply Voltage | TBD VDC |
| Differential Input Voltage | TBD V |
| Storage Temperature Range | –40°C to +125°C |
| Lead Temperature (Soldering) | +260°C |
| Output Short Circuit to Ground (+25°C) | Continuous |
| Junction Temperature ($T_J$) | +150°C |

***Figure 5. Receive Channel Timing***

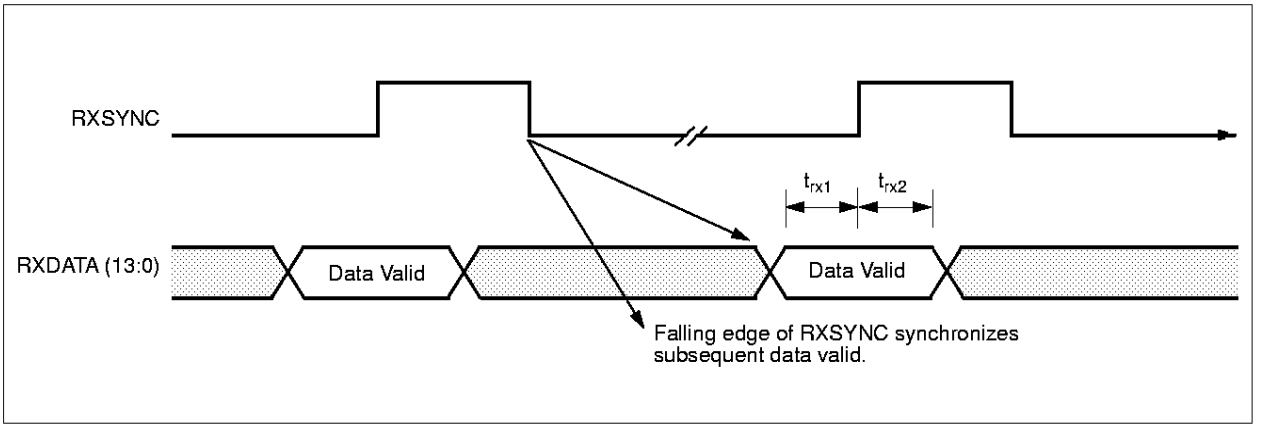
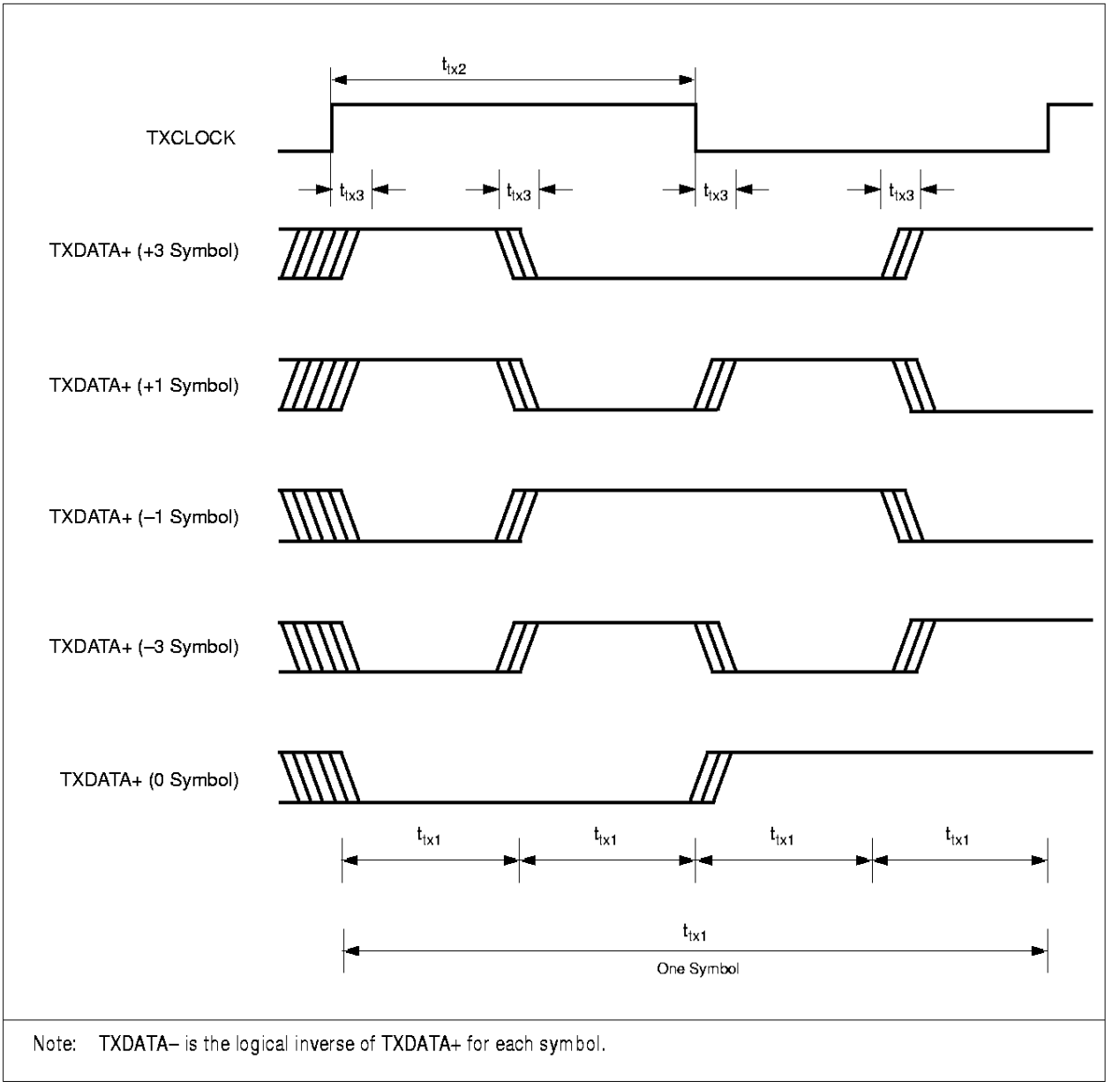


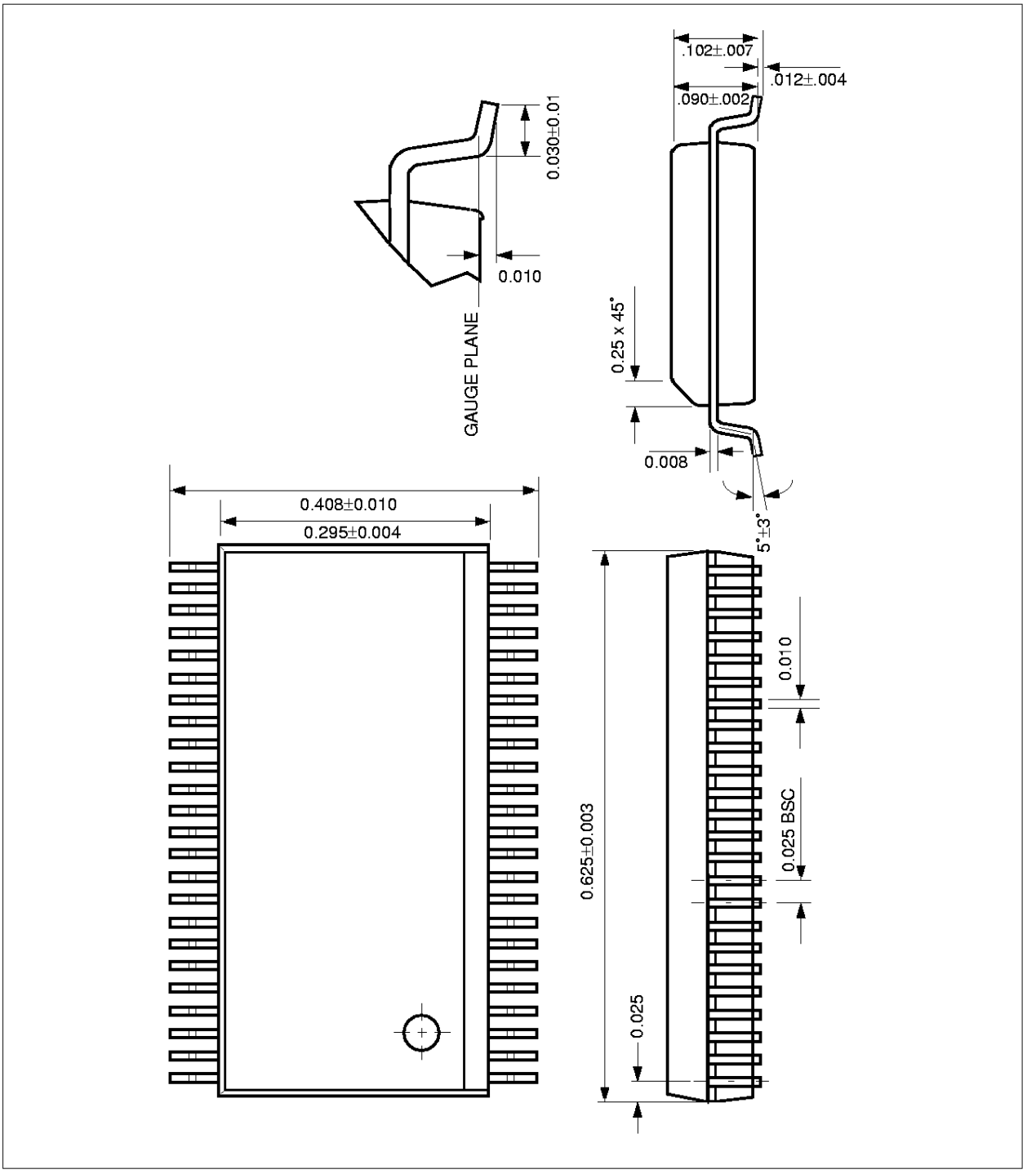
***Figure 6. Transmit Channel Timing***




Note: TXDATA– is the logical inverse of TXDATA+ for each symbol.

# *Mechanical Specifications*

***Figure 7. 48-Pin Shrink Small Outline Package (SSOP)***



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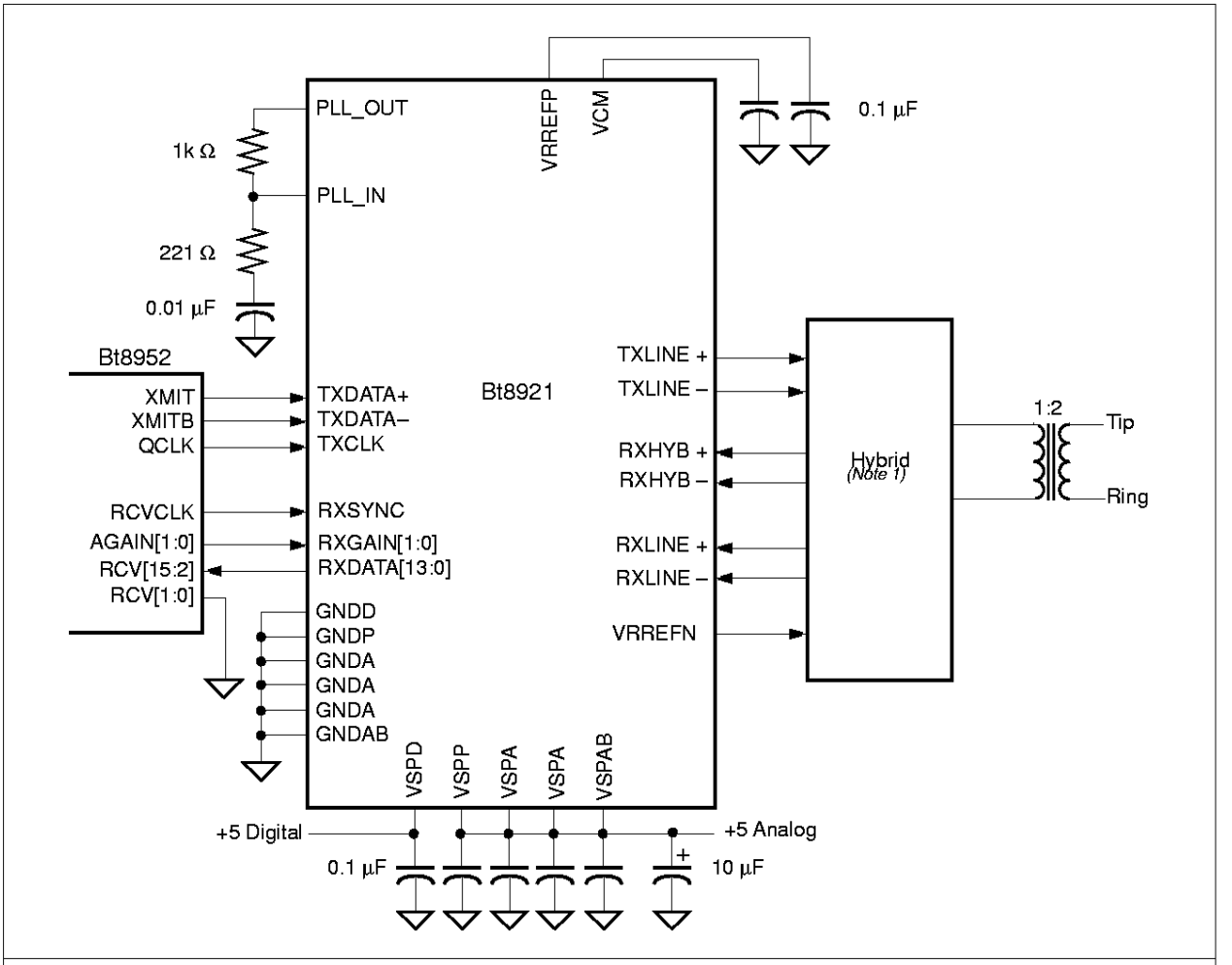
# Application Information

## Basic Bt8921 Interconnection Diagram

The basic interconnection diagrams for the Bt8921 are shown in Figures 8 and 9. Recommended component values are listed in Table 7.

*Figure 8. Basic Bt8921 Interconnection Diagram*




Note: See Figure 9 for Hybrid Configuration.

*Figure 9. Bt8921 Hybrid Configuration*

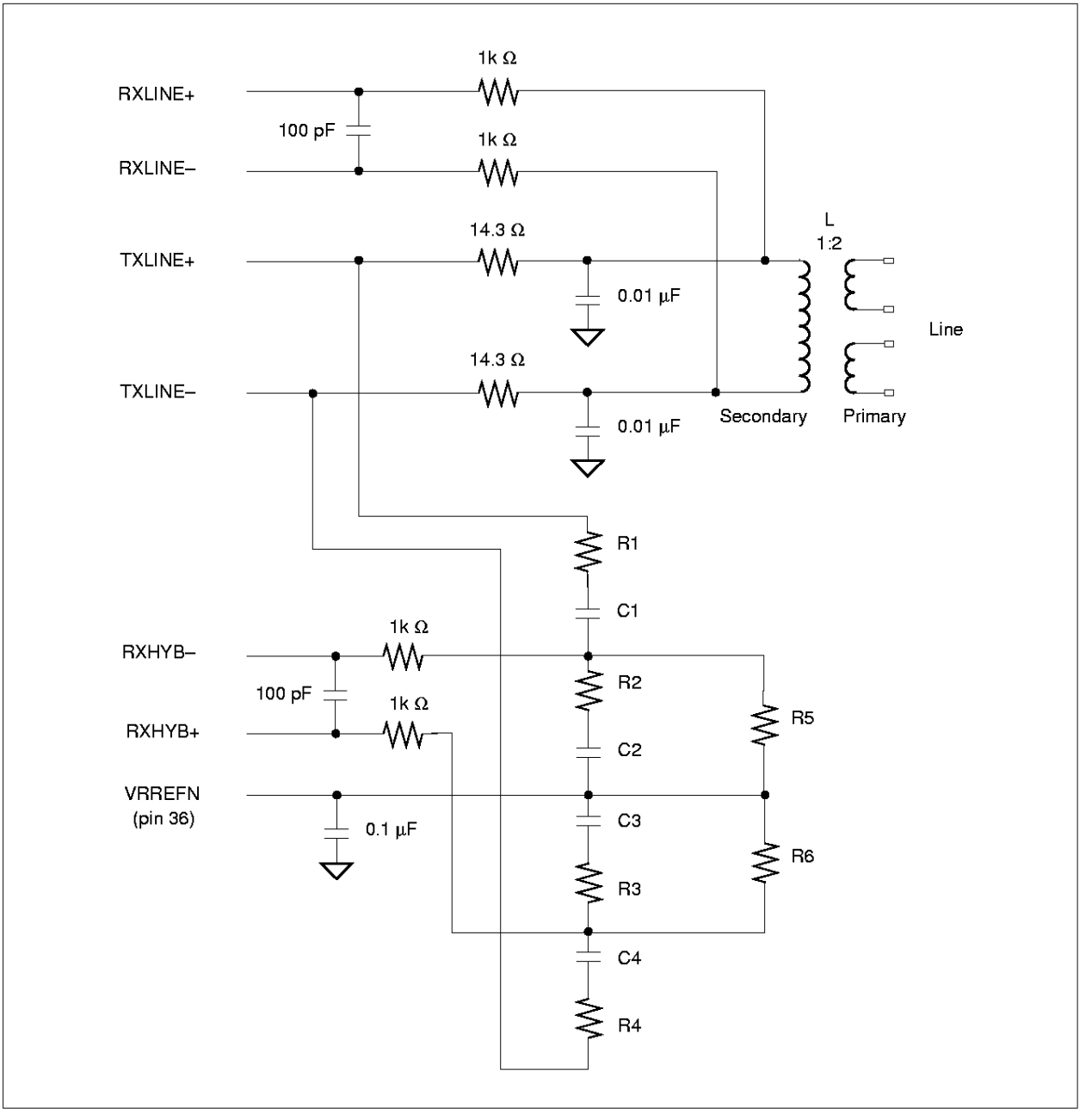


*Table 7. Hybrid Configuration Component Values*

| Hybrid Component | Data Rate | |
|---|---|---|
| | 1168 kbps | 784 kbps |
| R1, R4 | 1.3 k Ω | 1.3 k Ω |
| C1,C4 | 3 nF | 4.7 nF |
| R2, R3 | 1k Ω | 787 Ω |
| C2, C3 | 1 nF | 1.8 nF |
| R5, R6 | 6 k Ω | 6 k Ω |
| L (OCL) | 2 mH | 3 mH |

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